HARDWARE ACCELERATORS IN THE DESIGN AUTOMATION ENVIRONMENT

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The addition of hardware accelerators to design automation applications has been enthusiastically received by the engineering community. However, this new market raises novel issues which will be addressed in this panel.

The cost/peformance benefits of machines such as the MegaLOGICIAN, PMX, Zycad, RealChip, RealFast, and the Calay router prove the viability of pushing time consuming software algorithms down into specialized hardware. To determine the feasibility of using this approach for a particular product there are several issues engineers must consider, including:

- What product functions need to be accelerated?
- How general purpose should the accelerator be?
- How much should it cost?
- How fast should it run?
- How well can it be integrated within the user's existing design environment?

Performance Tradeoffs

As with any design problem, these constraints interact with each other in complicated ways.

Raw performance alone is not sufficient. For example, a two state logic simulator is useless no matter how fast it runs. To tailor the solution to meet customer needs, you must first fully understand the customer's problem.

For a given algorithm, a general purpose machine offers lower price/performance than a special purpose machine. However, overspecialization may lead to a product which cannot be upgraded as the algorithms it implements are refined. For example, a simulator implementing a nine state model may not be able to be upgraded to twelve states if the hardware is overspecialized. Tom Blank from Stanford University and Jack Kohn from IBM will provide insight into the general purpose vs. special purpose argument.

Additionally, a more general purpose piece of hardware may be able to accelerate other algorithms in the design enviroment. For example, a bit map machine may be able to handle both routing and DRC. Thus, a more general purpose architecture can reduce the total design time more than a single special purpose machine. Dave McCubbrey from the Enviromental Research Institute of Michigan will discuss the Michigan Enviromental approach, which ideally illustrates this tradeoff.

Integrating the Solution

Software development is frequently the bottleneck in integrating an accelerator into the design environment. If the primitive concepts of the algorithm do not map well to the operations supported by the architecture, integration may prove impossible. In addition, without adequate support tools from the vendor, development and maintenence of support software becomes the responsibility, headache, and bottleneck of the customer.

The implementation of hardware accelerators in the commercial environment will be discussed by Ram Banin of Daisy Systems, developers of the MegaLOGICIAN, and by Jack Goodhue of Bolt, Beranek, & Newman, the inventors of the butterfly machine.

Implementing specialized algorithms in hardware requires innovative design techniques such as custom VLSI, gate arrays and dataflow architecture. These solutions provide a large increase in performance while not significantly increasing cost. The speakers will discuss their choice of tradeoffs for each of their solutions.

0738-100X/84/0000/0648$1.00 © 1984 IEEE