The CHIP

Peak Detectors for Multistandard Wireless Receivers

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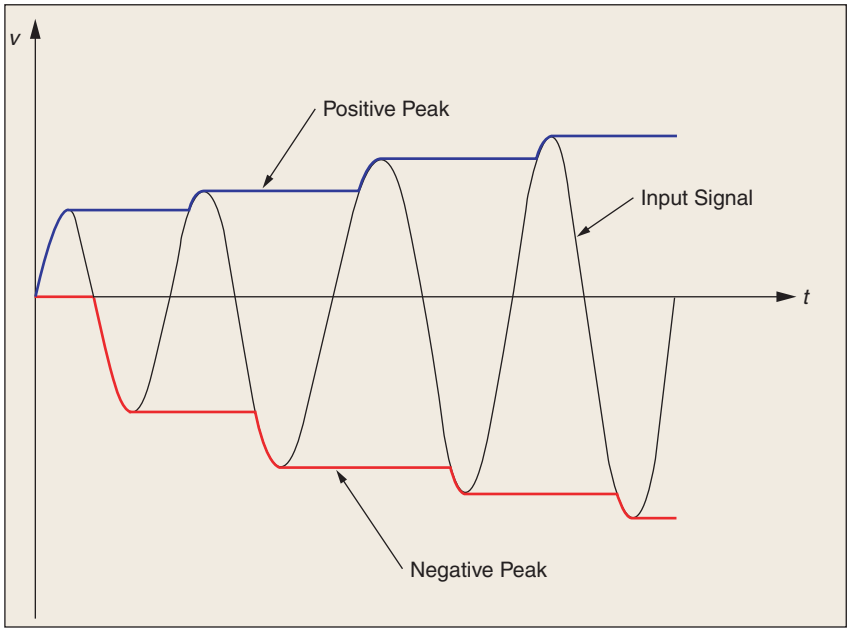
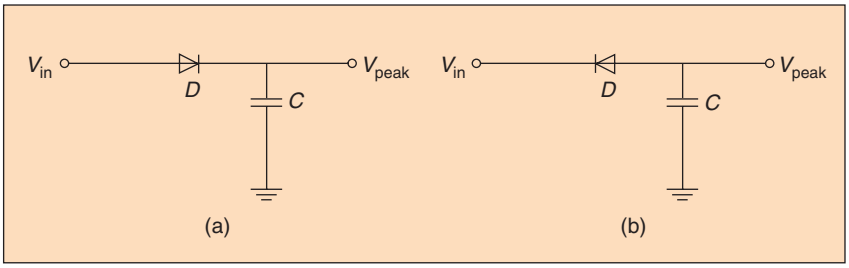
Peak detectors (or envelope detectors) are commonly found in modern communication receivers mainly as a building block of automatic gain control (AGC) loops. The main function of the peak detectors is to detect the peak value of an input signal and track the peak over time. A positive peak detector is to follow the maximum value of an input signal and a negative peak detector (or valley detector) is to trace the minimum value of the input signal. Figure 1 illustrates ideal peak detector outputs from both peak detectors. In this article, we present some of peak detector topologies and their applications in multistandard wireless receivers.



1. Ideal peak detector outputs.



2. Diode-capacitor peak detectors. (a) Positive peak detector (b) Negative peak detector.

PEAK DETECTOR TOPOLOGIES

The simplest positive peak detector is a diode-capacitor circuit as shown in Figure 2(a) and its negative counterpart with the diode reversed is in Figure 2(b) [1]. In the positive peak detector circuit in Figure 2(a), while the input voltage V_{in} is larger than the output peak voltage V_{peak} plus the diode voltage drop, the peak point of an input signal charges up the hold capacitor C and V_{peak} follows V_{in}. While V_{in} is smaller than the output peak voltage V_{peak} and the diode is reverse biased, the capacitor holds the value. Thus, this circuit cannot precisely track the input peak voltage because the output peak voltage is always less than the actual peak voltage by the diode voltage drop, and the circuit is insensitive to the peak less than the diode voltage drop. Therefore, this circuit is not suitable for detecting small signals. Furthermore, the diode voltage drop is dependent on temperature and current, which makes the circuit more inaccurate. Another drawback of this simple circuit is that the input impedance is variable and very low during forward biased condition. In addition, peak detectors have two major problems: droop and slew rate. The droop is a slow discharge from the hold capacitor through the leakage and the path provided by the following stage, and it makes the output peak voltage deviate from the true peak value. It is better to reduce the droop for accuracy. The slew rate is about the speed of charging the hold capacitor. It is better to increase the slew rate for speed. To increase the speed of the peak detector for tracing a fast input waveform, the

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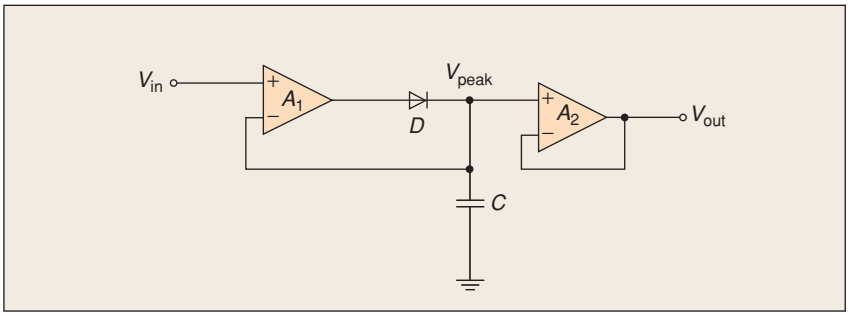
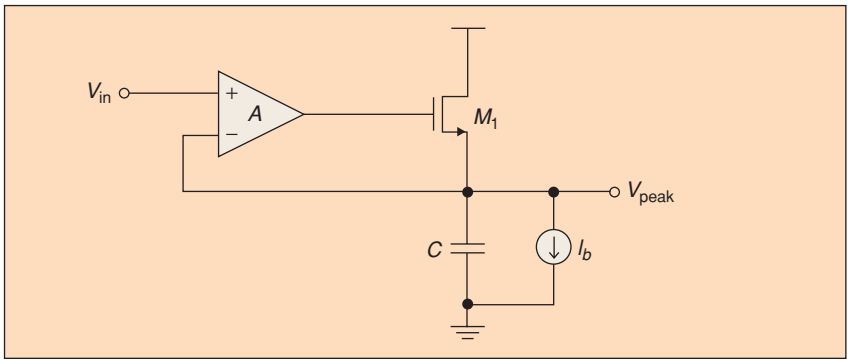
value of the hold capacitor should be reduced. However, the smaller capacitor will cause the larger droop because it can discharge quickly. Therefore, there is a trade-off between low droop rate and high slew rate in peak detector design. To improve performance, this basic peak detector topology can be modified in many ways [1].

A more practical positive peak detector topology using op-amp is shown in Figure 3 [1]. By feeding back the V_{peak} to the op-amp negative input, the diode voltage drop problem can be fixed because the loop around A_1 is closed through the diode D and the V_{peak} can closely trace V_{in} while V_{in} is larger than V_{peak}. On the other hand, while the V_{in} is less than V_{peak}, the output of A_1 goes to negative saturation with the loop open and the capacitor is holding the peak value. The output peak voltage is connected to a buffer (A_2) to isolate V_{peak} from the next stage. In this circuit, additional unwanted charging from the op-amp input bias currents can contribute to the droop so that MOSFET input devices should be utilized in both A_1 and A_2. Also, finite op-amp slew rate is limiting the speed. In a monolithic peak detector, the A_1 must be carefully designed to avoid a possible stability problem in a closed loop condition.

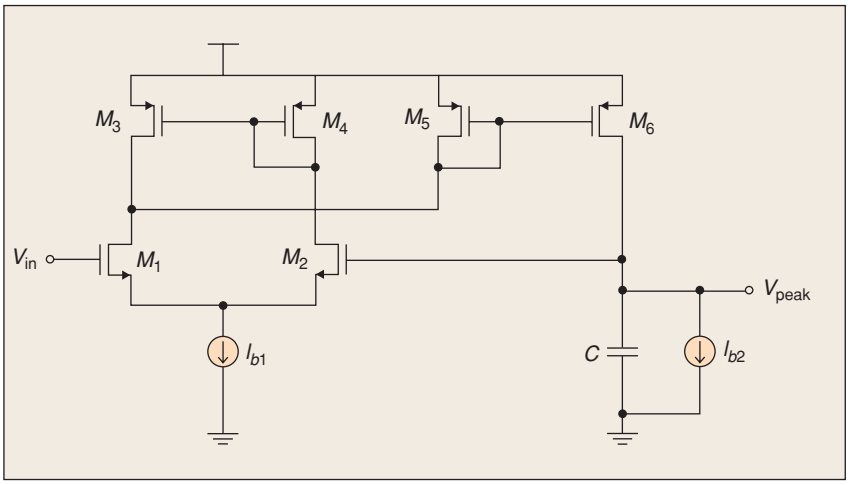
In integrated peak detector circuits, a diode can be implemented simply as a diode-connected MOS transistor [2], [3]. Or, a source follower [4], [5] can be employed to perform the diode function. Figure 4 shows a positive peak detector using a source follower. A buffer could follow the peak detector for isolation. While V_{in} exceeds V_{peak}, M_1 is on, which charges the capacitor C. While V_{in} goes below V_{peak}, M_1 is off and the capacitor holds the output peak voltage. A very small current source I_b is included to discharge the capacitor for better tracking. A resistor can be used instead of a current source. So, the droop rate is controlled by the capacitance as well as the current source. That is, the droop rate (dV_{peak}/dt) is given by I_b/C since $I = C$ (dV_{peak}/dt) across the capacitor. In designing an AGC loop, this droop rate should be carefully determined to meet the AGC settling requirement. In addition, parasitic capacitors should be considered to see if the leakage current can affect the droop rate. A low droop rate peak detector could discharge slowly while the envelope of an input signal keeps decreasing faster below the previous peak voltage, in which case the V_{peak} cannot follow the V_{in} fast enough. Thus, we need to reset the peak detector periodically so that it can quickly follow the next input peak point. A reset mechanism can be implemented with a simple NMOS switch across the hold capacitor C which zeros the output instantly.



3. Positive peak detector using op-amp.

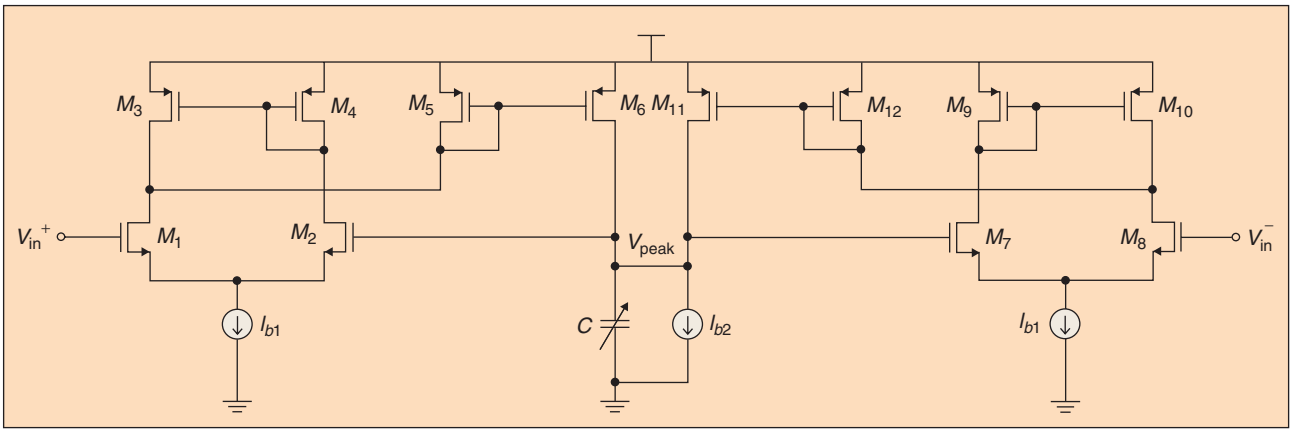


4. Positive peak detector using source follower.

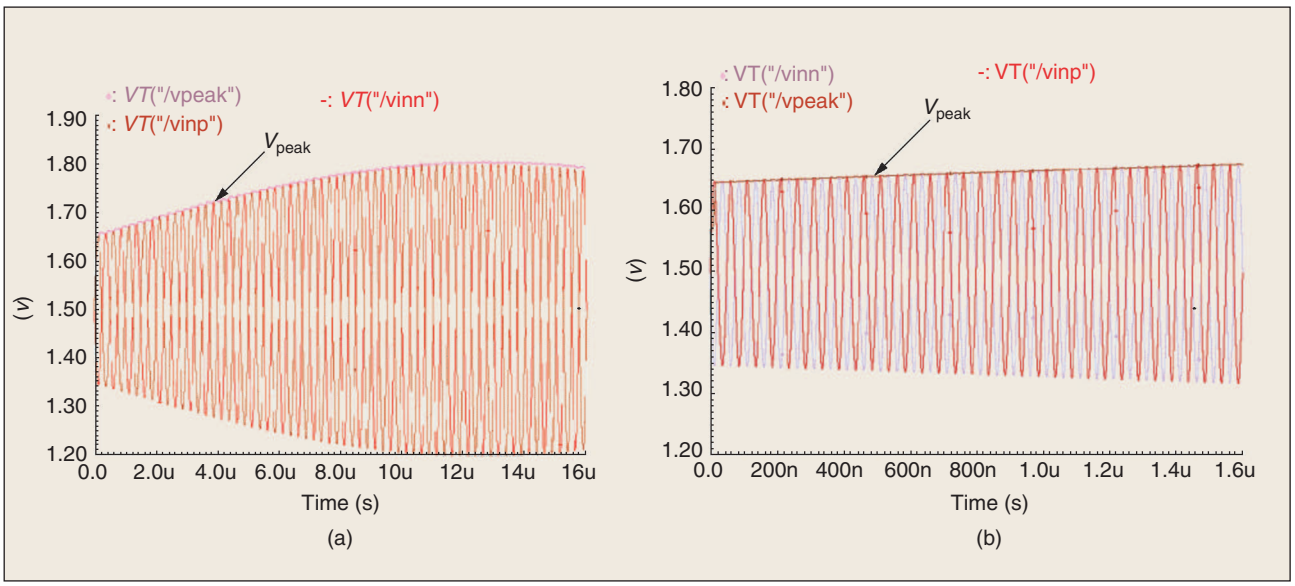


5. Positive peak detector using current mirror.

Interestingly, a diode can be replaced with a current mirror [6], [7]. As shown in Figure 5, a positive peak detector is constructed with a differential amplifier ($M_1 \sim M_4$) and a current mirror (M_5 and M_6). If the V_{in} is larger than the V_{peak}, the excess current is flowing through M_5 which is also copied to M_6 and charging the hold



6. Differential positive peak detector.



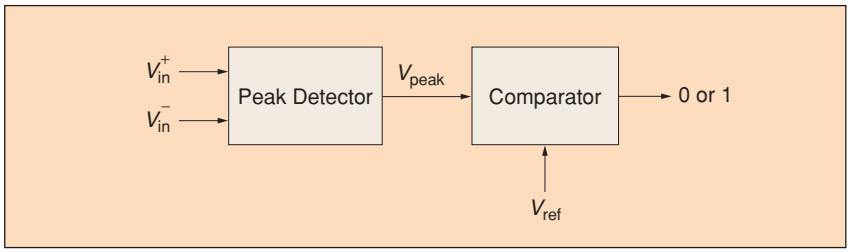
7. Simulation results of differential peak detector in Figure 6. (a) With 2 MHz input signal. (b) With 20 MHz input signal.

capacitor C. The small current source I_{b2} is for discharging. We can control the droop rate of the peak detector by adjusting the values of capacitance and the current source.

In designing a peak detector, the values of the hold capacitor and the current source are optimized to accurately detect the peak of a certain input signal. Therefore, it is difficult to make a peak detector work for a wide range of input frequencies. In order to design a peak detector for multistandard wireless receivers, we need to make the peak detector process a broader range of input signals. Figure 6 shows one realization of a peak detector for multistandard receivers which is a differential version of the positive peak detector using current mirror in Figure 5. Both positive and negative differential input signals are fed to two identical positive peak detectors, and a hold capacitor and a current source are shared. The single-ended output peak voltage is thus the maximum of the two peak voltages. Here, to make it work for more than one wireless standard, the capacitor C can be made variable by using switches. Figure 7 shows the simulation results of the differential peak detector with two capacitors connected with switches and switching current source I_{b2}. Figure 7(a) is the result with 2 MHz input signal and Figure 7(b) is with 20 MHz input signal. Those input signals are amplitude-modulated with modulation frequency 20 KHz and modulation index 1. By switching the hold capacitor and the current source simultaneously, the peak detector can efficiently detect the two input signals with different frequencies.

APPLICATION

A peak detector is a key building block in a received signal strength indicator (RSSI). The RSSI is required for an automatic gain control (AGC) loop in wireless communication receivers. The RSSI detects the peak of an input signal normally at the input of a variable gain amplifier (VGA) and compares it with a certain threshold voltage to produce a digital level output. Using the RSSI output, the AGC controls the gain setting of low noise amplifiers and VGAs. Figure 8 shows a simple one bit RSSI architecture consisting of a peak detector and a comparator. The final RSSI output is either 0 V or V_{DD}. The peak detector was



8. Simple RSSI architecture.

implemented with a differential peak detector shown in Figure 6. In the peak detector, a reset switch (which was not drawn in the figure) was also included across the hold capacitor C to quickly respond to the variation of the peak. A comparator with hysteresis was designed to improve immunity to the noise at the peak detector output. The supply voltage was 3.3 V. The simulation result of the RSSI is shown in Figure 9. The reset switch was on for 384.6 ns from 30 µsec to cut the slow decay.

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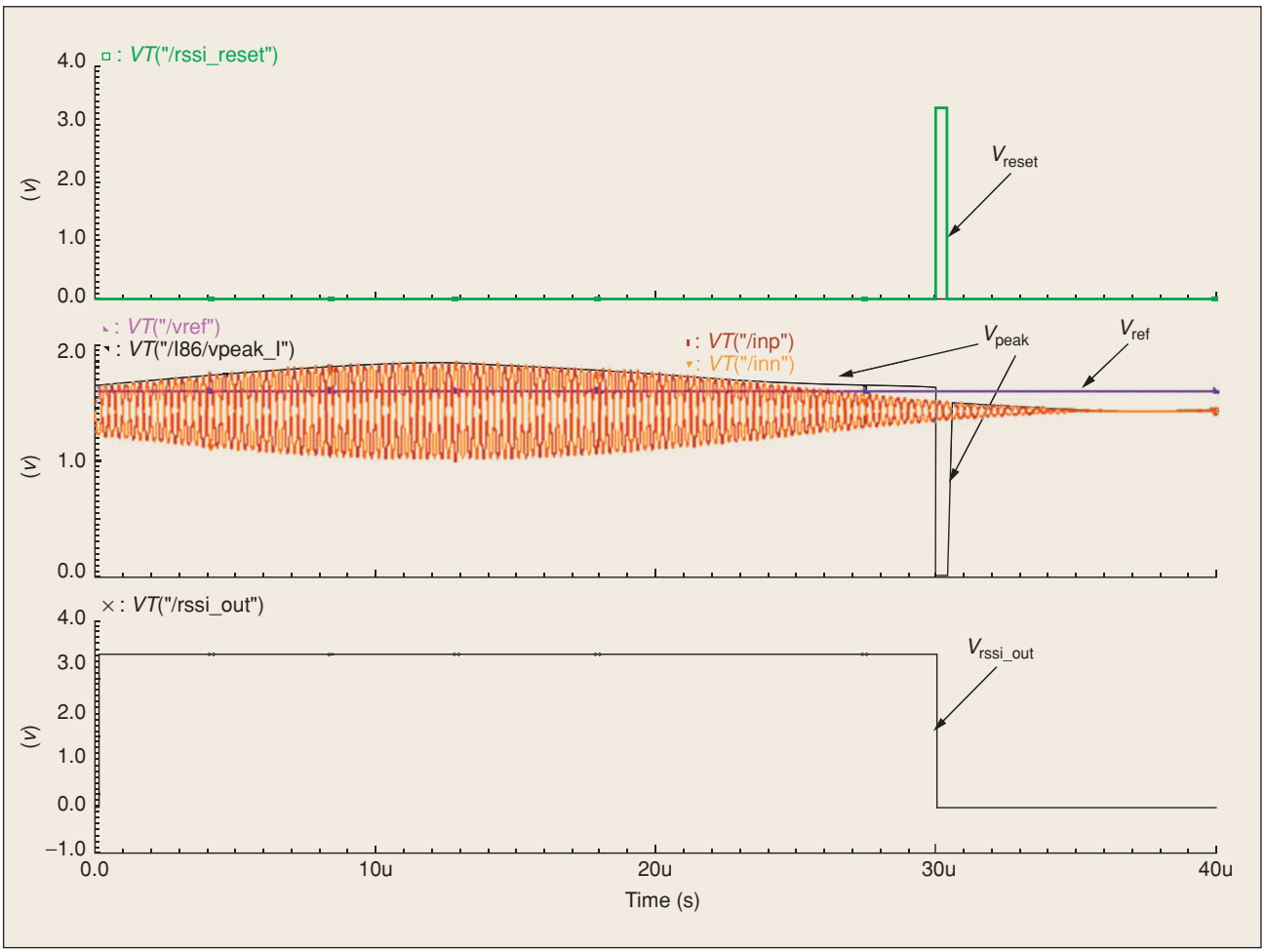

9. Simulation result of RSSI in Figure 8.