Guest Editorial
Special Section on Field Programmable Gate Arrays

FIELD programmable gate (FPGA's) have become an important technology for the design and implementation of VLSI circuits and systems since their invention in the mid-1980's. The field programmability and reprogrammability of FPGA's lead to many interesting and promising applications, such as fast implementation of application-specific integrated circuits, rapid system prototyping, circuit emulation, reconfigurable system designs, and reconfigurable computing. The steady increase of FPGA density and speed in the past ten years have made these applications feasible and economical. The fast growing FPGA industry and the widespread use of FPGA technology has resulted in an active research community, with a great deal of research activity in many areas including FPGA architecture and circuit design, FPGA design tool and algorithm development, and FPGA applications.

In order to provide a forum for researchers and developers in industry and academia to exchange ideas and results in the field of FPGA's, two International Workshops on FPGA's were organized in 1992 and 1994 under the sponsorship of ACM SIGDA. In 1995, this workshop became the annual International Symposium on FPGA's under the sponsorship of ACM SIGDA, held every February in Monterey, CA. It has become the premier forum for the presentation of advances in all areas related to FPGA technology.

This Special Section is devoted to recent research results on FPGA technology, with an emphasis on providing timely and in-depth presentations of the significant contributions reported in the 1997 ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA'97). After a careful review process, nine papers were selected from a total of 35 submissions. The papers in this Special Section are organized into three groups: FPGA Architectures and Systems, FPGA Synthesis and Layout, and FPGA Applications.

The three papers on FPGA Architectures and Systems show the range of ways that FPGA technology can have an impact on system-building. The first paper by Lewis *et al.* presents a system based on FPGA's that allows the user to quickly and easily construct prototype hardware systems with as many as 1 million gates. With this system, the architect can explore and analyze many more alternatives than possible with conventional technology. The second paper by Tsutsui and Miyazaki describes how FPGA circuits can be combined with a conventional processor architecture to produce a hybrid system that is both flexible and fast. This paper discusses how communications applications can be partitioned on such a system to take advantage of the most appropriate implementation. The third paper by Lach *et al.* describes how a high level of fault-tolerance can be achieved by using the reconfigurability of the underlying FPGA technology. By using the ability of FPGA's to implement arbitrary circuits, this technique avoids the cost incurred by fault-tolerance methods that rely on redundancy.

Three papers on FPGA Synthesis and Layout were selected for this Special Section. The paper by Wood and Rutenbar presents an interesting approach to FPGA routing via Boolean satisfiability. Given a netlist, a description of the routing fabric, a region to be routed, and the boundary constraints (determined by a global router), the method automatically generates a Boolean equation, whose satisfiability decides the routability of this region, and each of its satisfiable truth assignments, if any, specifies a routing solution. The Boolean satisfiability problem was solved using the ordered binary decision diagram representation. The short paper by Boemo *et al.* investigates the possibility of wave pipelining in FPGA designs. It presents a set of interesting experimental results, and shows that using wave pipelining, a 13-LUT logic depth circuit mapped on an XC4005PC84-6 can run as fast as 85 MHz (single phase clocking) or 80 MHz (intentionally skewed clocking) with a latency of 95 ns. Such a high throughput/latency ratio was not attainable using classic pipelining. The paper by Legl *et al.*, which will appear in the September 1998 issue, presents a novel functional decomposition algorithm that computes encoding functions with minimal inputs so that the number of look-up tables (LUT's) needed to implement a complex function can be reduced after such a decomposition. It has the unique feature of computing a set of encoding functions implicitly and then choosing the ones with the minimal support. The algorithm is efficient and yields substantial reduction of the number of LUT's on MCNC benchmark circuits.

The three papers on FPGA Applications present recent research results on using FPGA's in novel ways. The paper by Von Herzen shows that very high-performance circuits can be achieved with FPGA's by using a combination of appropriate architecture and careful design. This paper presents a complete design and implementation of a cross correlator that runs at 250 MHz. The paper by Wirthlin and Hutchings presents a careful analysis of run-time reconfiguration as a general technique for reducing the resources required by an application. The authors present several examples of using run-time reconfiguration and analyze the overhead of reconfiguration relative to its benefits. The paper by Chia *et al.*, which will appear in the September 1998 issue, describes using FPGA's to accelerate the correlation computation required by a target recognition application. This system uses a combination of an application-specific architecture implemented with FPGA's and reconfigurability to share the same hardware for different functions. This application is an excellent example of the benefits of the new paradigm of configurable computing.

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Dr. Cong served as the General Chair of the 4th ACM/SIGDA Physical Design Workshop, the Program Chair and General Chair of the 1997 and 1998 International Symposium on FPGA's, and as a Program Committee member of many VLSI CAD conferences, including DAC, ICCAD, and ISCAS. He is an Associate Editor of *ACM Transactions on Design Automation of Electronic Systems*. He received the Best Graduate Award from the Peking University in 1985 and the Ross J. Martin Award for Excellence in Research from the University of Illinois at Urbana-Champaign in 1989. He received the NSF Research Initiation Award and NSF Young Investigator Award in 1991 and 1993, respectively. He received the Northrop Outstanding Junior Faculty Research Award from UCLA in 1993 and the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS Best Paper Award in 1995.

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