Scanning the Issue

Special Issue on Quantum Devices and Their Applications

The ability to use geometry scaling to improve the performance/cost ratio of electronics has fueled the Age of Information. As we approach the next millennium, the end of the Great Device Shrink appears to be at hand [1], and it is appropriate and intriguing to speculate about the future of electron device technology. Basic physical length scales, including atomic bond lengths and the electron wavelength, are even today being approached in MOSFET's. Accounting for the quantum effects associated with these nanometer device dimensions is becoming an important aspect of device design. This Special Issue focuses on the increasing "quantum" content of electronics in the twenty-first century.

Every device is, of course, a quantum device, operating according to the laws of quantum mechanics, but devices with nanometer feature sizes display the quantum of electron charge and the wave properties of matter, e.g., interference, resonance, diffraction, and tunneling, in remarkable and strong ways. For the purposes of this Special Issue, we consider quantum devices to be nanometer-scale electron devices. Starting from complimentary metal-oxidesemiconductor (CMOS) technology, we have placed an emphasis in this issue on technologies which could find a significant niche apart from CMOS or augmenting CMOS. Each of the authors has been asked not only to outline their respective fields, but also to assess the prospects for future application.

Fig. 1 provides a rough outline of the six papers and six technology areas discussed in this issue, along with an estimate of when these technologies might be expected to emerge. With no clear successor to CMOS technology looming, CMOS should dominate the marketplace into the next century. What we can expect for CMOS as it moves to the nanometer scale is the subject of the paper by Wong *et al.* entitled "Nanoscale CMOS."

Tunneling devices in combination with silicon or III–V transistors offer a way to extend the performance of existing technologies by increasing circuit speed and decreasing static power dissipation. Both memory and logic benefits can be expected, and these subjects respectively are covered

Publisher Item Identifier S 0018-9219(99)02671-7.

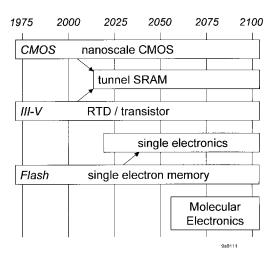


Fig. 1. Overview of this Special Issue on Quantum Devices and Their Applications. The timeline gives a guess at when the technology will find use. Each row of the chart is the subject of a paper in this issue. Acronyms: CMOS, static random access memory (SRAM), and resonant tunneling diode (RTD).

in the next two articles: "Tunneling-Based SRAM" by van der Wagt and "A New RTD-FET Logic Family" by Mathews *et al.*

The limiting size electron device, whose operation is based on the transport of individual electrons, has been the subject of significant study over the past decade. In this Special Issue, two papers outline progress and prospects for this field. The first paper, "Single-Electron Devices and Their Applications" by Likharev, covers the overall subject of single electronics. The second paper, by Yano *et al.*, covers the particular case of "Single-Electron Memory for Giga-to-Tera Bit Storage."

Lastly, we have a paper by Reed, which outlines one corner of an emerging area of research, "Molecular-Scale Electronics," a field that has been called the "final technological stage in the miniaturization of computer circuitry" [2]. With the enormous range of possibilities for molecular and biomolecular devices, it seems likely that molecular electronics will find significant applications in the twentyfirst century.

0018-9219/99\$10.00 © 1999 IEEE

REFERENCES

- [1] The National Technology Roadmap for Semiconductors. Austin, TX: Semiconductor Industry Association, 1997.
- [2] R. R. Birge, "Introduction to molecular and biomolecular electronics," in *Molecular and Biomolecular Electronics* (Advances in Chemistry Series 240), R. R. Birge, Ed. New York: American Chemical Society, 1994, ch. 1, pp. 1–14.

ALAN C. SEABAUGH, *Guest Editor* Raytheon Systems Company Dallas, TX 75266 USA

PINAKI MAZUMDER, *Guest Editor* University of Michigan Ann Arbor, MI 48109-2122 USA



Alan C. Seabaugh (Senior Member, IEEE) received the B.S., M. S., and Ph.D. degrees in electrical engineering from the University of Virginia, Charlottesville, in 1977, 1979, and 1985, respectively.

He is an Engineering Fellow in the Applied Research Laboratory of Raytheon Systems Company, Dallas, TX. He joined Texas Instrument's Central Research Laboratory in 1986 and has worked to develop nanoelectronics and high-speed transistor technology, including resonant tunneling diodes, bipolar and unipolar resonant tunneling transistors, and technologies for integrating high-speed resonant tunneling diodes with heterojunction bipolar and high electron mobility transistors. In 1991, he was elected Senior Member of Technical Staff; he was elected Distinguished Member of Technical Staff in 1997. In 1997 he joined Raytheon, where he is developing 10–100-GHz mixed-signal technology and silicon-based resonant tunneling devices. From 1979 to 1986, he was employed by the Electron Device Division of the National Bureau of Standards. He has authored or coauthored more than 100 papers and holds 16 U.S. patents.

Dr. Seabaugh is a member of the American Physical Society.



Pinaki Mazumder (Fellow, IEEE) received the B.S.E.E. degree from the Indian Institute of Science, Bangalore, in 1976, the M.Sc. degree in computer science from the University of Alberta, Canada, in 1985, and the Ph.D. degree in electrical and computer engineering from the University of Illinois, Urbana-Champaign, in 1987.

Presently, he is a Professor with the Department of Electrical Engineering and Computer Science of the University of Michigan, Ann Arbor. Prior to this he was a Research Assistant with the Coordinated Science Laboratory, University of Illinois, Urbana-Champaign, for two years and was with the Bharat Electronics Ltd. (a collaborator of RCA), India, for over six years, where he developed several types of analog and digital integrated circuits for consumer electronics products. During the summers of 1985 and 1986, he was a Member of the Technical Staff in the Indian Hill branch of AT&T Bell Laboratories. During 1996–1997, he spent his sabbatical leave as a Visiting Faculty Member at Stanford University, Stanford, CA, University of California, Berkeley, and Nippon Telephone and Telegraph, Japan. His research interests

include very large scale integration (VLSI) testing, physical design automation, and ultrafast circuit design. He is the co-author of two books: Testing and Testable Design of High-Density Random-Access Memories (Kluwer, 1996) and Genetic Algorithms for VLSI Design, Layout and Test Automation (Prentice-Hall, 1999).

Dr. Mazumder served as the Guest Editor of the March 1998 Special Issue on Emerging Nanoelectronic Technologies and Their Applications of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS and is an Associate Editor of that same publication. He is a recipient of Digital's Incentives for Excellence Award, a BF Goodrich National Collegiate Invention Award, a National Science Foundation Research Initiation Award, and a Bell Northern Research Laboratory Faculty Award. He is a member of Sigma Xi, Phi Kappa Phi, and ACM SIGDA.